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GB 2166899 A EP 0484062 A1 US 4994896 A
US 4724531 A

(58) Field of Search
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(54) Integrated circuit having mirror-image pin assignments

(57) A circuit assembly has at least one IC mounted on opposing sides of a board by utilizing one or more IC's having pin assignments (1 - 208) arranged as a mirror image of each other along a centreline through the IC package such that one or more IC's (610, 660 and 615, 665) having the same set of mirror image pin assignments mounted on each side of a circuit board and rotated 180 degrees in relationship to each other will ensure that the pin assignments of the same type will be directly opposite each other and separated by the circuit board. The IC's may also be mounted on opposite surfaces of the board such that their pin assignments are aligned (Fig. 6, not shown). A plurality of pins having non-mirror image assignments may also be present on the IC's.

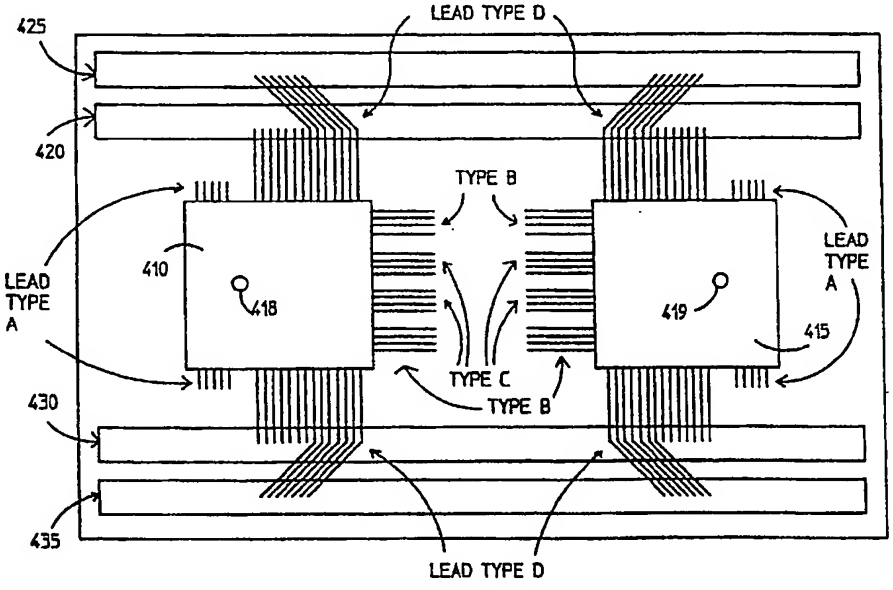

FIG 4

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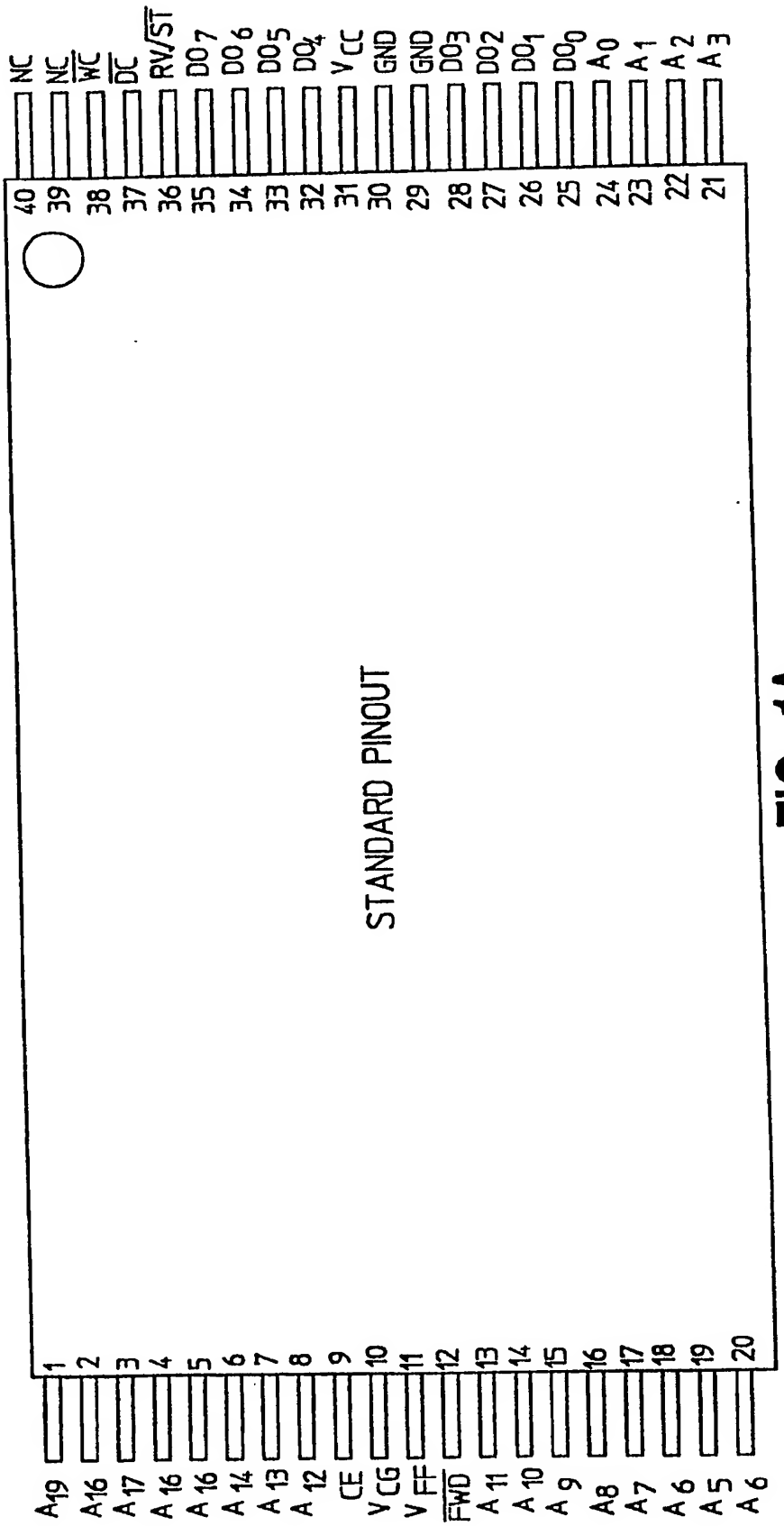


FIG 1A

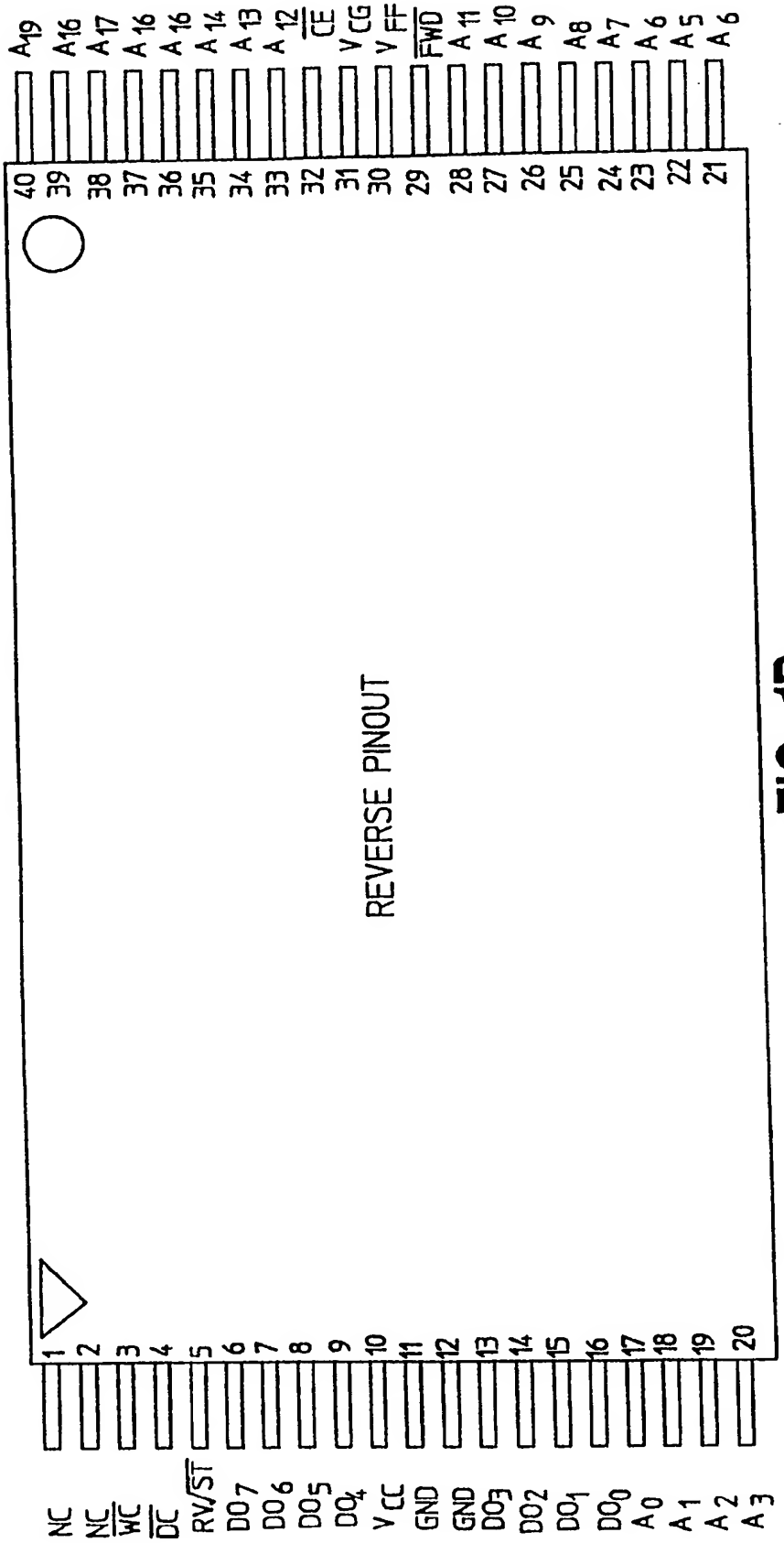


FIG 1B

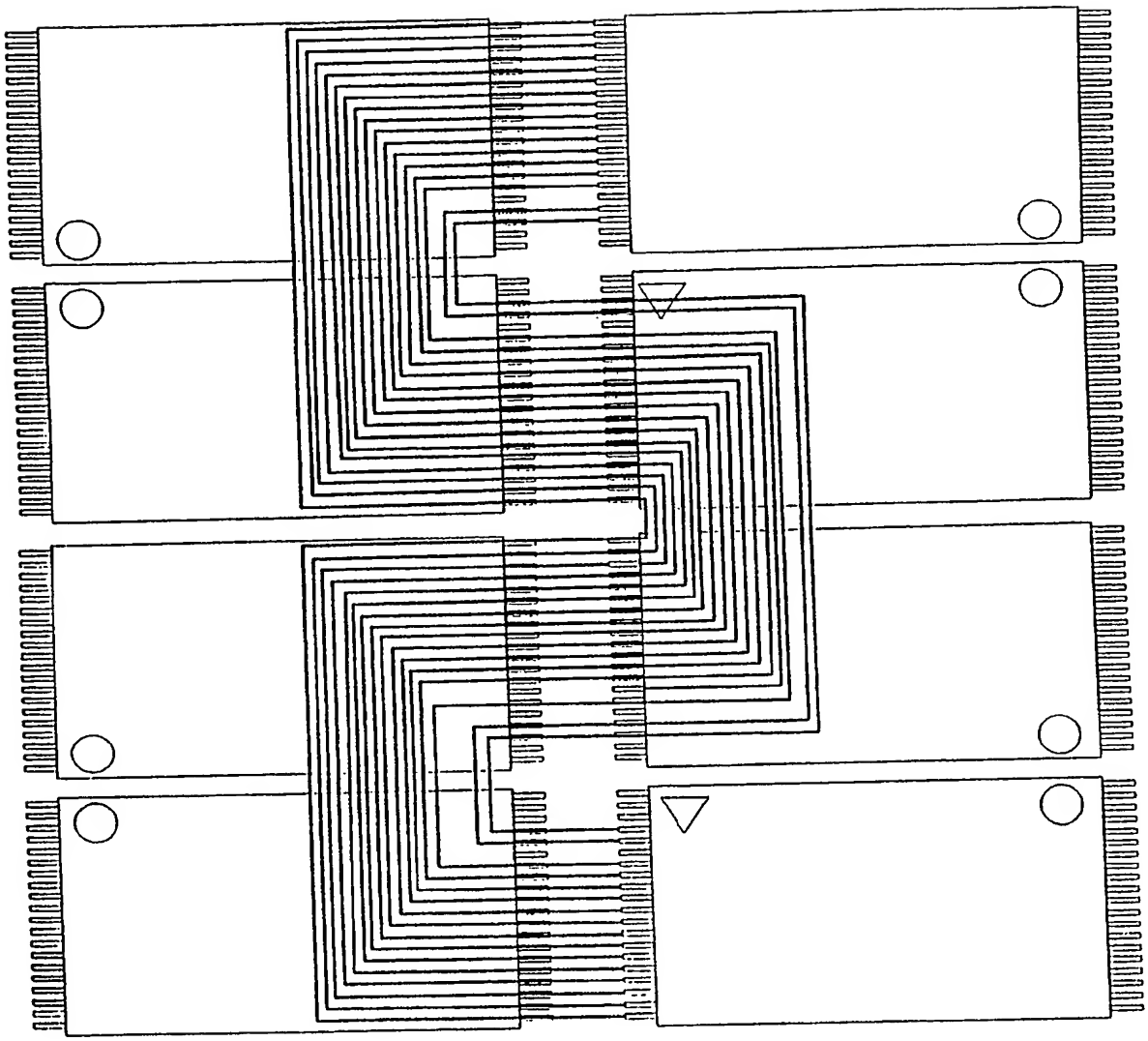


FIG 2

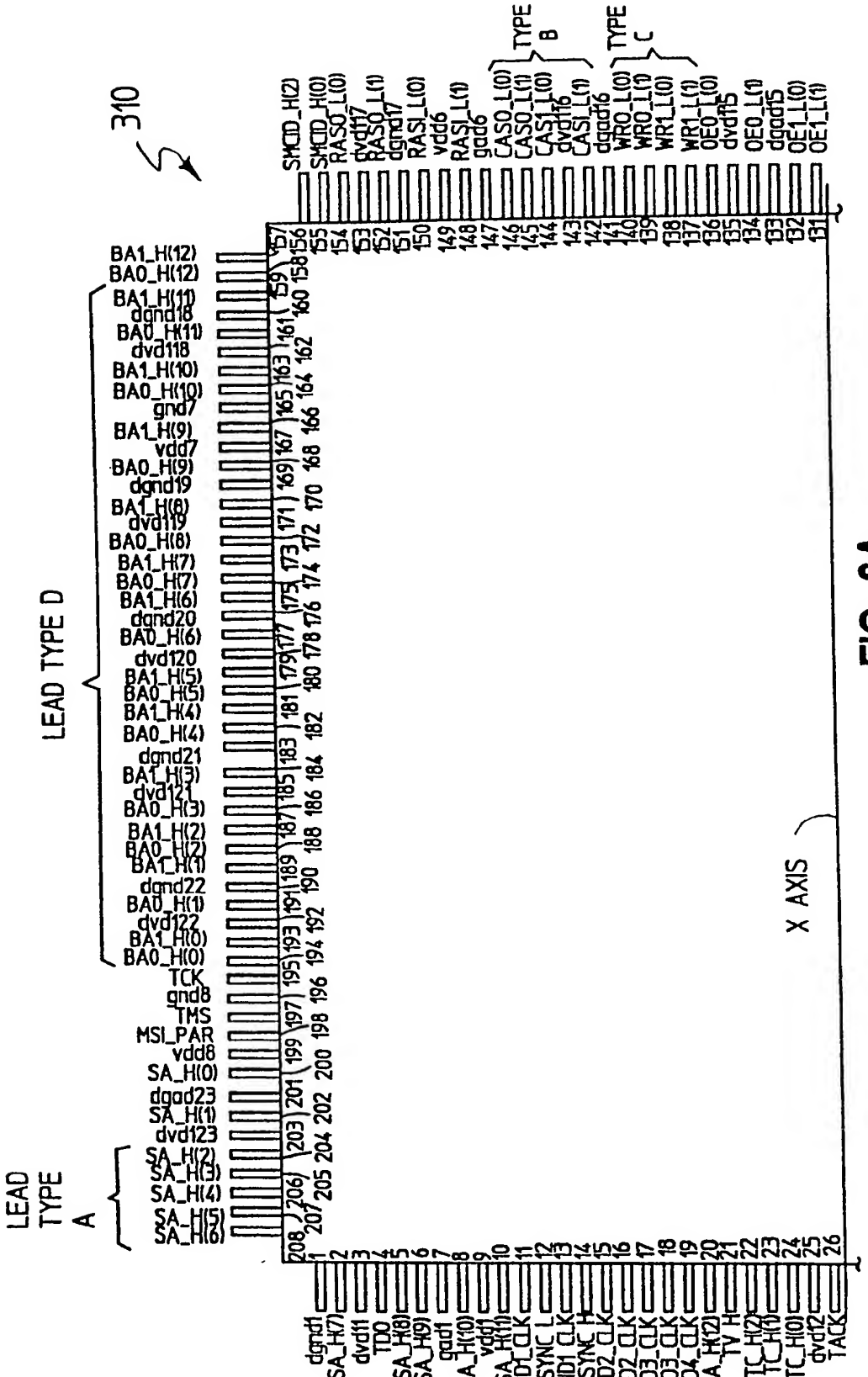


FIG 3A

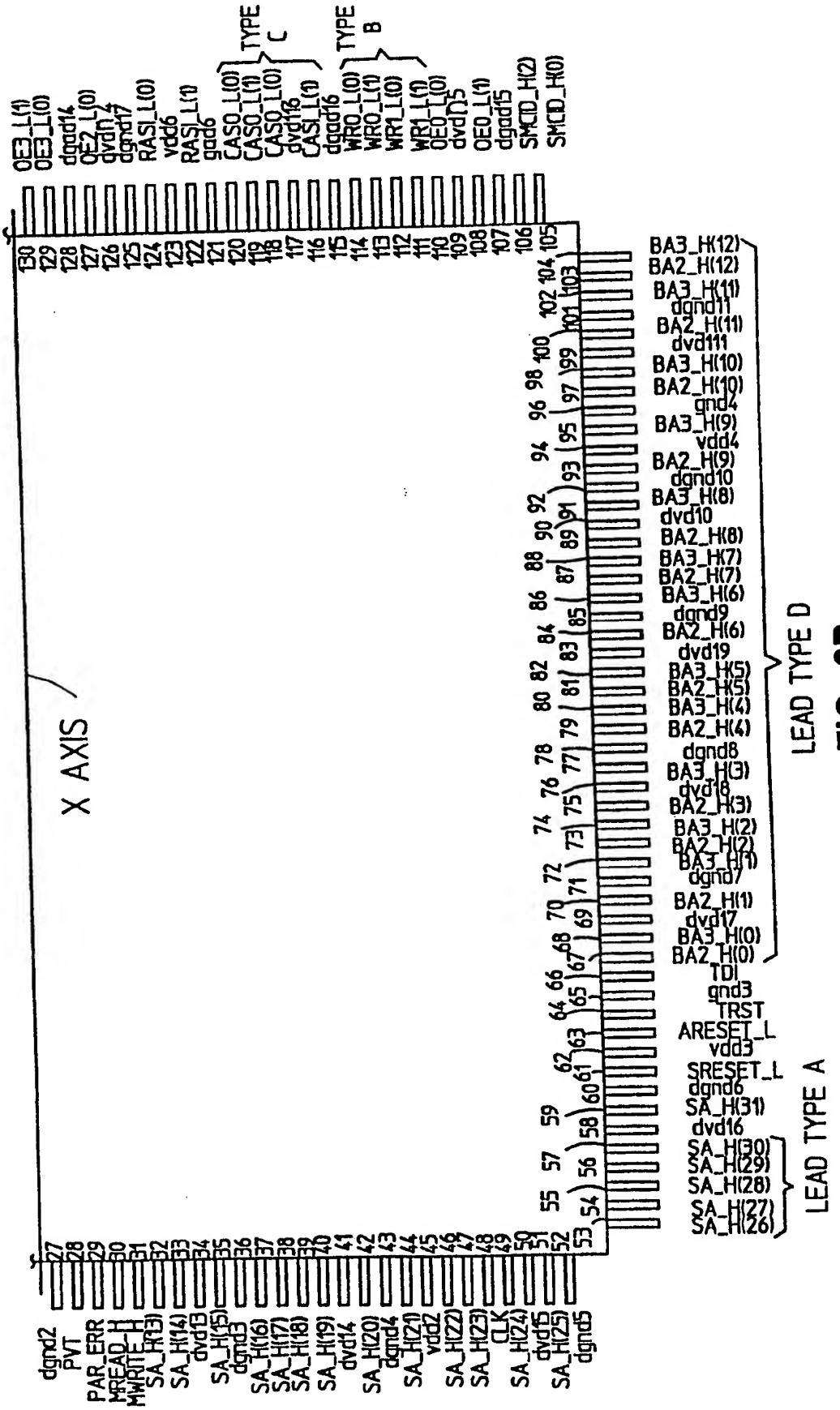


FIG 3B

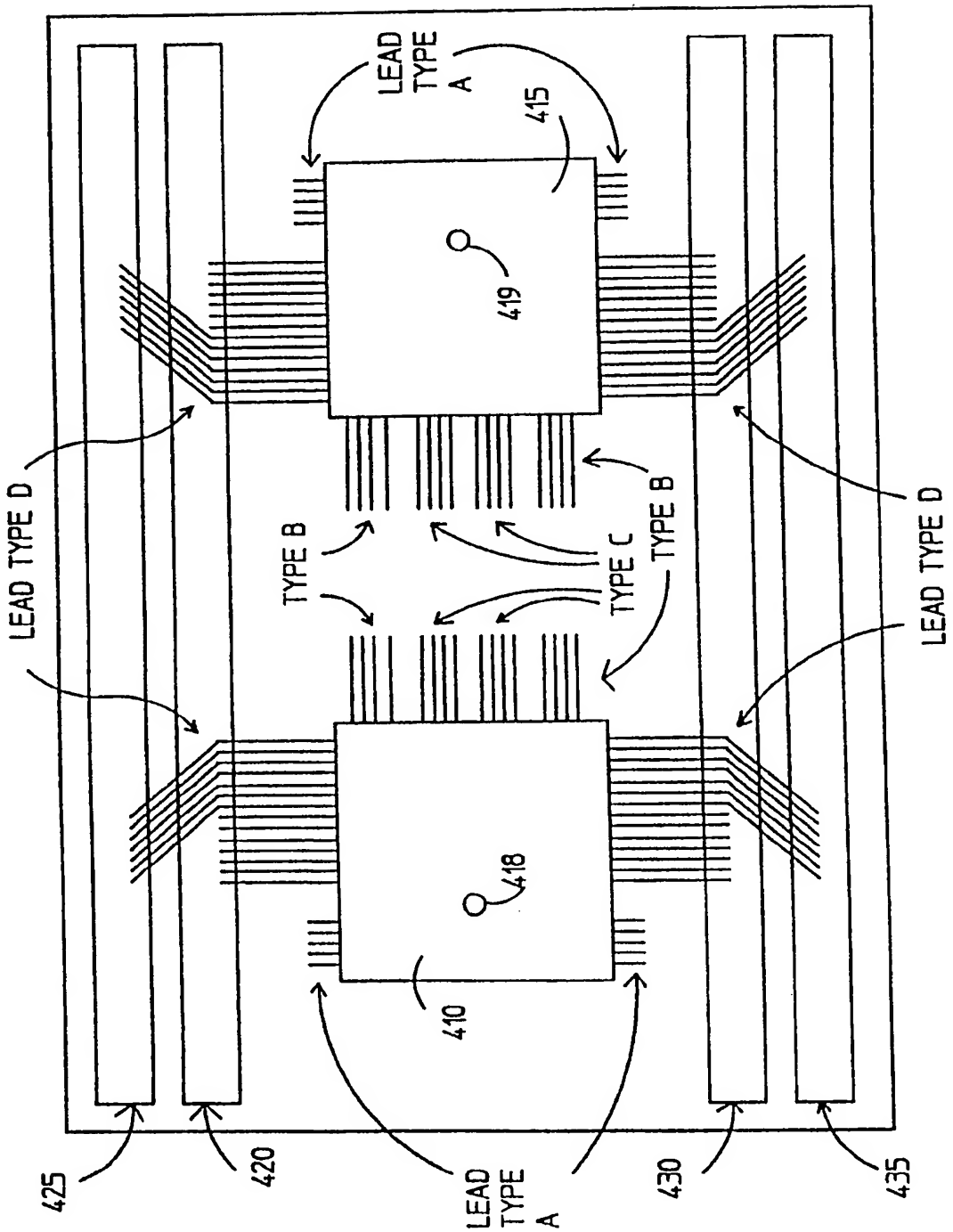


FIG 4

FIG 5

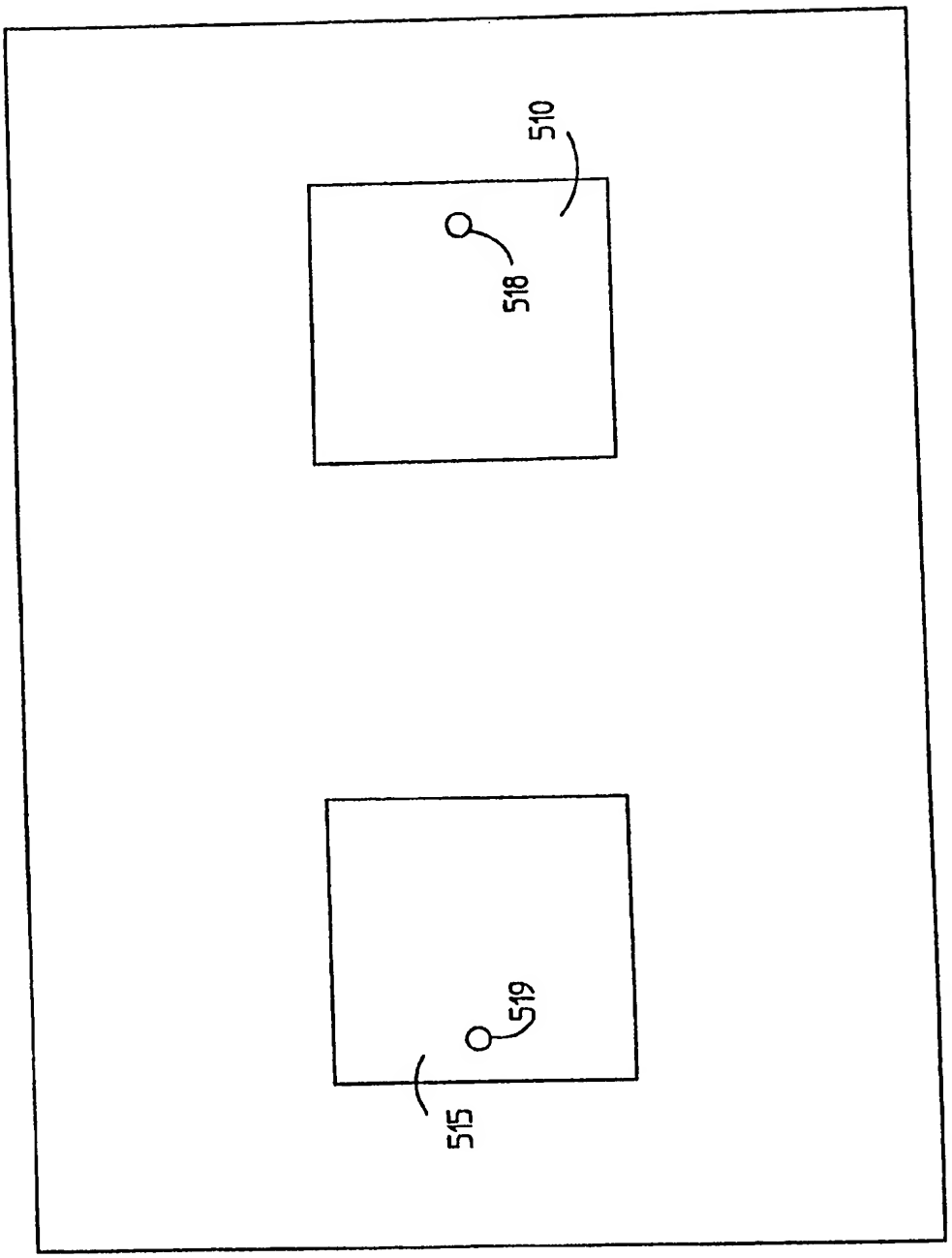
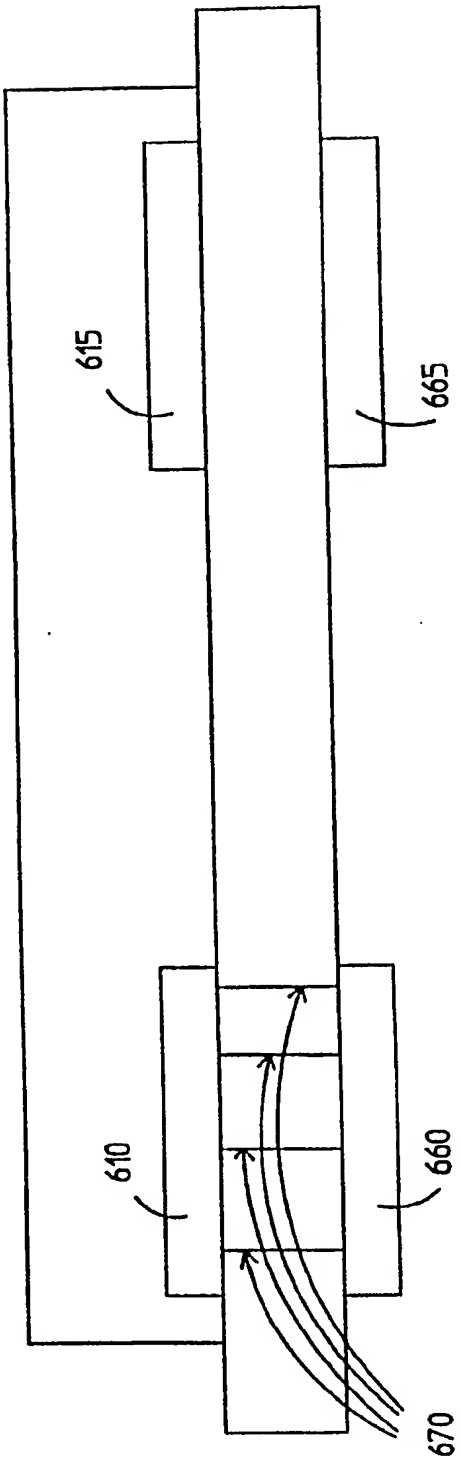


FIG 6



CIRCUIT BOARD ASSEMBLY AND CHIP PACKAGE THEREFOR

The present invention relates to integrated circuit design and, more particularly, to an integrated circuit package, to a circuit board assembly and to a method of routing leads on a circuit board assembly.

Lead routing between Integrated Circuits (IC's) on a Printed Circuit (PC) board plays an important role in both the cost and the performance of the PC board design. The cost of manufacturing a PC board is directly related to the number of layers required to effectively route all of the leads between the IC's. The ability to reduce the number of leads, match the length of leads and the potential for interference between leads enhances the performance of the PC board. As the IC density on PC boards increases and the number of pin assignments and associated leads per IC go up, lead routing becomes increasingly more difficult.

In the mid-80's, surface mount technology (SMT) and double sided SMT were introduced as an alternative to standard through-hole PC board technology. Instead of pre-drilling PC boards to accept the pins of IC's, special packaging for IC's was developed which provided for gluing IC's to the PC board. Since the requirement for sticking pins through to the opposite side of the PC board and soldering the IC's in place was eliminated, it became possible to mount IC's on both sides of the PC board.

Even though SMT provides for increased efficiency in

lead routing, problems still exist as the total number of IC's on the PC board doubles with two-sided SMT. The number of leads required to interconnect IC's goes up with both the total number of IC's on the PC board, as well as with advances in Very Large Scale Integration (VLSI) design (up to 1,000,000 components may now be integrated into a single IC). A standard 1 megabyte memory chip has 44 pin assignments, a custom memory controller chip may have over 200 pin assignments, and a multichip module (MCM) which approaches 2.5 centimeters square may have over 500 pin assignments.

The layout of a circuit board generally proceeds from the circuit diagram to a geometric layout in which IC's are grouped in their respective isolation regions. Leads coupling IC's are laid out to eliminate potential lead crossovers. Lead routing is a three dimensional problem and becomes very complex with high chip and associated lead densities. Lead crossovers are typically eliminated by adding additional layers to the circuit board such that leads can be re-routed through vias to different levels. Via is the term used to describe a hole partially through the circuit board which enables a lead to travel from one board level to another. Additionally, lead routing is made even more complex as constraints such as maximum length and a consistency between lead lengths must be provided for.

As circuit speeds increase the distributed capacitance and inductance over the length of each lead

causes it to act like a transmission line. Reduction of the overall lead length reduces adverse electronic emissions from the circuit board. Crosstalk (an undesirable coupling between an active line and an adjacent passive line) may occur do to mutual inductance or capacitance. Crosstalk can also cause a loss of signal strength in the active line, and interference or false triggering in an adjacent line. Lateral crosstalk may occur when adjacent leads are located on the same plane. Leads located on opposite sides of a dielectric laminate may result in vertical crosstalk. Crosstalk can be minimized by increasing the distance between adjacent leads or reducing the length of parallel lead sections. Vertical crosstalk can be virtually eliminated by orthogonal routing of leads on adjacent layers.

In circuit boards incorporating more than one IC of the same type, circuit board complexity, problems associated with crossover and crosstalk, can be minimized by utilizing pairs of integrated circuits designed with two identical but reversed pin assignments. As illustrated in Figure 1, an eight MBIT Flash memory sold by Intel (F28F008SA) is offered in both a standard pin assignment (Figure 1A) and a reversed pin assignment (Figure 1B) configuration. By alternating the memory chips in a serpentine layout (Figure 2), the reversed pin assignment provides for a greatly simplified board layout as crossovers and the length of the interconnecting leads are minimized. Unfortunately, two different IC's must be

manufactured and proper placement on the PC board necessitates subsequent identification during IC insertion.

Another example of the prior art is disclosed in U.S. Patent No. 5,270,964 issued December 14, 1993 to Bechtolsheim et al. Bechtolsheim discloses a single in-line memory module (SIMM) having two hundred pin assignments. A high number density connector is used to connect the SIMM to a memory module socket on a PC board. All power and ground leads are symmetrically arranged within the connector. Power and ground leads alternate every sixteen pins such that if the SIMM is inadvertently inserted in a reversed position into the memory module socket, the symmetrical power and ground leads prevent the SIMM from being reverse-powered, and likely destroyed.

The present invention seeks to provide improved circuit board assemblies.

According to an aspect of the present invention, there is provided an integrated circuit package for mounting to a circuit board comprising a plurality of pin assignments arranged as a mirror image around the periphery of said package and positioned as a mirror image of each other along an axis drawn through the centre of said IC package; and a plurality of non-mirror image pin assignments.

According to another aspect of the present invention, there is provided a circuit board assembly as herein defined, wherein said first and second integrated circuit

packages are rotated 180° relative to one another so as to have adjacent mirror image pin assignments.

According to another aspect of the present invention, there is provided a method of routing leads on a circuit board assembly comprising the steps of providing first and second mirror image integrated circuit packages each having pin assignments positioned as a mirror image of each other along an axis drawn through the centre of said package, mounting the first circuit package to a top side of the circuit board, mounting the second circuit package to a bottom side of the circuit board such that said first and second circuit packages are rotated 180 degrees relative to one another, mounting at least one additional integrated circuit package of a different type to the top side of said circuit board, said additional integrated circuit having some pin assignments which are identical to pin assignments of said first and second circuit packages, coupling a first set of leads between mirror pin assignments of said first circuit package and said additional integrated circuit package, coupling a second set of leads between mirror pin assignments of said second circuit package and said additional integrated circuit package, said first and second set of leads following the same general direction on the circuit board.

It is possible to provide with some embodiments simplified lead routing and a reduction in the number of layers in the board required to accommodate the demands of high density ICs and multichip modules having hundreds of

pin assignments.

It can also provide for increased IC density on circuit boards having at least one IC mounted on each side of a two sided PC or SMT board. One or more ICs may be designed such that pin assignments are arranged as a mirror image of each other along a centerline through the IC package in an X or Y axis. One or more IC's having the same set of mirror image pin assignments may be mounted on each side of a circuit board. Rotating each integrated circuit by 180 degrees in relationship to an integrated circuit already positioned directly on the opposite side of the circuit board can ensure that the pin assignments of the same type will be directly opposite each other and separated by the circuit board.

Lead routing may be greatly simplified as leads emanating from pin assignments of the same type (on opposite sides of the circuit board) can be routed in the same direction and are less likely to have crossover related problems. Lead lengths for similar types of leads between two ICs may be more easily maintained within requisite length tolerances. Additionally, two ICs directly opposite each other on either side of the circuit board may have identical pin assignments (such as ground and power) and may be coupled together through the circuit board for twice the current flow.

While it is generally not possible to ensure that all pin assignments have a mirror image counterpart, routing can be simplified even when only a small plurality of pin

assignments have a mirror image counterpart. As the number of ICs having mirror image pin assignments increases, the advantages are magnified. Preferably, a substantial number of the pin assignments have a mirror image counterpart.

Where an IC is not operated at the same time as an IC positioned opposite it, only one set of leads will be transmitting information and as a result crosstalk between leads on opposite sides of the circuit board can be minimized.

An embodiment of the present invention is described below, by way of example only, with reference to the accompanying drawings, in which:

Figure 1A is a plan view of a prior art IC having a standard pin assignment and Figure 1B is a second IC having a reversed pin assignment.

Figure 2 is a plan view of a prior art PC board layout incorporating the prior art IC's of Fig.1 in a symmetrically blocked architecture.

Figures 3A and 3B are a plan view of a preferred embodiment of mirror image IC.

Figure 4 is a plan view of the top of a preferred embodiment of circuit board layout.

Figure 5 is a plan view of the bottom of a preferred embodiment of circuit board layout of Figure 4.

Figure 6 is a cross-sectional view of the preferred embodiment of circuit board of Figure 4.

Figures 3A and 3B illustrate a preferred embodiment

of integrated circuit, which in this example is a slave memory controller IC chip 310 having a pin assignment mirrored in the X axis. In particular, ground lead 1 (dgnd1) is at pin assignment 1 located in the top left corner of the IC. Mirrored down to the bottom left corner is ground lead 5 (dgnd5) at pin assignment 52. Various ground, power, data, strobe, clock and address leads around the chip package have pin assignments which are positioned as a mirror image of each other. Where possible, these pin assignments are grouped together to further reduce the possibility of lead crossover. Most IC's have multiple numbers of pin assignments of the following types; address, data, column address strobe, row address strobe, error correction, write enable, reset and power. Mirror image counterparts are formed by locating, around the IC package, pin assignments of each type an equal distance from the centerline.

In the preferred embodiment, lead type A located across the top left corner and bottom left corner of the IC package defines a group of 6 SA_ pin assignments and a ground pin assignment, lead type B located halfway up the right upper and lower half of the IC package defines a group of four column address strobe (CAS) signals and a power pin assignment (dvd). lead type C is also located on the right side but closer to the x axis centerline and defines for write (WR) pin assignments and lead type D is located across most of the top and bottom of the IC package and defines 26 address lines BA on each side.

Figure 4 illustrates the top view of SMT board 400 having two identical memory controller chips 410 and 415 mounted between SIMM module bank 420 and SIMM module bank 430. All of which are mounted between SIMM module bank 425 and SIMM module bank 435. As denoted by circular marker 418 and circular marker 419, memory controller chip 415 is rotated 180 degrees in relationship to memory controller chip 410. Since the sets of type B and sets of type C pin assignments located equidistant from the X axis, similar types of leads are directed towards each other. A plurality of leads couple the pin assignments from the memory controller chips to the SIMM modules 425 and 435.

Figure 5 is a view of the bottom side of the SMT board illustrated in Figure 4. Memory controller chip 515 is mounted directly opposite memory controller chip 410 of Figure 4, however, note that it is now located on the right side of the SMT board (whereas memory controller chip 410 is mounted on the left side) and as denoted by the circular marker 518, memory controller chip 510 is rotated 180 degrees from its top side counterpart such that their pin assignments and associated lead routings match. Memory controller chip 515 is now on the left side and as denoted by the circular marker 519, memory controller chip 515 is rotated 180 from its top side counterpart. Furthermore, leads not illustrated couple the pin assignments from the memory controller chips 510 and 515 to SIMM modules 420 and 430 on the opposite side

of the PC board. The leads pass through vias to lower levels such that connections can be made to the SIMM modules mounted on the top side of the PC board. Lead routing is greatly simplified as leads emanating from pin assignments of the same type (on opposite sides of the circuit board) are routed in the same direction and are less likely to have crossover related problems. Lead lengths for similar types of leads between two IC's are easily maintained within requisite length tolerances as the routings are very similar. Additionally, where two pin assignments located directly opposite each other on either side of the circuit board are identical (such as ground (grd) and power (dvd)) they may be coupled together through the circuit board for twice the current flow.

Figure 6 illustrates how the memory controller chips 610 and 615 are mounted directly opposite memory controller chips 660 and 665. The inherent mirror image of the pin assignments of the memory controllers ensure that the back to back pin assignments will be very similar. Such similarity makes lead routing easier as leads which typically go in the same direction will not have to crossover each other. Additionally, identical leads such as ground and power may be coupled together through circuit board vias 670 for increased current flow.

The disclosures in United States patent application no. 08/221,144, from which this application claims priority, and in the abstract accompanying this application are incorporated herein by reference.

Claims

1. An integrated circuit package for mounting to a circuit board comprising a plurality of pin assignments arranged as a mirror image around the periphery of said package and positioned as a mirror image of each other along an axis drawn through the centre of said IC package; and a plurality of non-mirror image pin assignments.

2. An integrated circuit package as claimed in claim 1, wherein said pin assignments are grouped together by type.

3. An integrated circuit package as claimed in claim 1 or 2, wherein a plurality of said mirror image pin assignments are identical pin assignments.

4. An integrated circuit package as claimed in claim 3, wherein said identical pin assignments comprise ground pin assignments.

5. An integrated circuit as claimed in claim 3 or 4, wherein said identical pin assignments comprise power pin assignments.

6. A circuit board assembly comprising first a circuit board onto which are mounted integrated circuit packages according to any preceding claim, wherein said first and second integrated circuit packages are rotated 180° relative to one another so as to have adjacent mirror

image pin assignments.

7. A circuit board assembly as claimed in claim 6, wherein said first integrated circuit package is mounted on a top side and said second integrated circuit package is mounted on a bottom side of said circuit board.

8. A method of routing leads on a circuit board assembly comprising the steps of providing first and second mirror image integrated circuit packages each having pin assignments positioned as a mirror image of each other along an axis drawn through the centre of said package, mounting the first circuit package to a top side of the circuit board, mounting the second circuit package to a bottom side of the circuit board such that said first and second circuit packages are rotated 180 degrees relative to one another, mounting at least one additional integrated circuit package of a different type to the top side of said circuit board, said additional integrated circuit having some pin assignments which are identical to pin assignments of said first and second circuit packages, coupling a first set of leads between mirror pin assignments of said first circuit package and said additional integrated circuit package, coupling a second set of leads between mirror pin assignments of said second circuit package and said additional integrated circuit package, said first and second set of leads following the same general direction on the circuit board.

9. A method as claimed in claim 8, wherein said mirror image pin assignments are grouped together by type.

10. A method as claimed in claim 8 or 9, wherein some of said mirror image pin assignments are identical and positioned such that said identical pin assignments are directly opposite each other when said first and second packages are mounted on opposing sides of the circuit board.

11. An integrated circuit package substantially as hereinbefore described with reference to and as illustrated in Figures 3A to 6 of the accompanying drawings.

12. A circuit board assembly substantially as hereinbefore described with reference to and as illustrated in Figures 3A to 6 of the accompanying drawings.

13. A method of routing leads on a circuit board assembly substantially as hereinbefore described with reference to Figures 3A to 6 of the accompanying drawings.

Patents Act 1977 Examiner's report to the Comptroller under Section 17 -14- (The Search report)	Application number GB 9504765.0
Relevant Technical Fields (i) UK Cl (Ed.N) H1K-KRE;H1R-RAA (ii) Int Cl (Ed.6) H01L-23/495;H05K-1/18	Search Examiner S J DAVIES Date of completion of Search 2 JUNE 1995
Databases (see below) (i) UK Patent Office collections of GB, EP, WO and US patent specifications. (ii) ONLINE WPI, INSPEC	Documents considered relevant following a search in respect of Claims :- ALL

Categories of documents

X:	Document indicating lack of novelty or of inventive step.	P:	Document published on or after the declared priority date but before the filing date of the present application.
Y:	Document indicating lack of inventive step if combined with one or more other documents of the same category.	E:	Patent document published on or after, but with priority date earlier than, the filing date of the present application.
A:	Document indicating technological background and/or state of the art.	&:	Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages		Relevant to claim(s)
X,Y	GB 2166899 A	(HITACHI) see eg Figure 4	X: 1 at least Y: 8 at least
X	EP 0484062 A1	(MITSUBISHI) see eg Figure 1	6
X,Y	US 4994896	(UEMURA ET AL) see Figures 6, 7	X: 6, 7 Y: 8 at least
X,Y	US 4724531	(ANGLETON ET AL) see eg Column 3 lines 55 - column 4, line 18	X: 1 at least Y: 8 at least

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